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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,939	01/16/2004	Craig Hansen	43876-153	4645

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EXAMINER
MOLL, JESSE R

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
10/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,939	HANSEN ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12 July 2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been examined.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9 July 2007 has been entered.

Information Disclosure Statement

3. The information disclosure statement filed 12 July 2007 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. All documents which have not been considered are either missing, unreadable, or improperly labeled.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ito et al. (U.S. Patent No. 5,742,782), herein referred to as Ito et al.'782.

6. Referring to claim 1, Ito et al.'782 discloses, as claimed, a programmable processor (see Fig. 1) comprising: a data path (comprising execution parts 25a-25d, see Fig. 1) capable of transmitting data (inherently, a data path is capable of transmitting data); an external interface operable to receive data from an external source (certainly existing in Ito et al.'782's system for handling input/output operation for peripherals) and communicate the received data over the data path; a register file containing a plurality of registers (register parts 26a-26c, see Fig. 1) each having a register width (including at least 173 and 174, see Fig. 6), the

register file coupled to the data path and operable to support processing of a plurality of threads (Threads A, B, and C, see Fig. 3) and to store a plurality of data elements in partitioned fields (each bit in the data registers), each of the data elements having an elemental width smaller than the register width (1 bit); an execution unit (execution parts 25a-25d, see Fig. 1) coupled to the data path, the execution unit operable to execute a plurality of instruction streams from the plurality of threads (Threads A, B, and C, see Figs. 3 and Fig. 15A), each instruction stream including a single instruction that specifies an operation (any FixOp instruction) to cause multiple instances of the operation to be performed (such as ADD or OR; these operations are merely operations repeated on every bit of the integer), each instance of the operation to be performed using a different one of the plurality of data elements (data area 173, see Fig. 6) in partitioned fields of at least one of the registers (single bits in the FixOp register 26c, see Fig. 1) to produce a catenated result, each of the data elements (data area 173, see Fig. 6).

Note claims 8, 13, and 20 recite the corresponding limitations as set forth above in claim 1. Ito et al.'782 also discloses as to Claims 8 and 20 first and second registers (register parts 26a-26c, see Fig. 1).

7. As to claim 2, Ito et al.'782 also discloses: the processor of claim 1 wherein the execution unit (execution parts 25a-25d, see Fig. 1) comprises a pipeline (see Fig. 15B) having a plurality of stages and wherein the pipeline interleaves execution of instructions (such as A1-A12, B1-B10, and C1-C10, see

Fig. 15A) from the plurality of instruction streams. Claims 9, 14, and 21, recite the corresponding limitations as set forth above in claim 2.

8. As to claim 3, Ito et al.'782 also discloses: the processor of claim 2 wherein the pipeline is operable to simultaneously contain states of execution of at least two instructions (such as A1-A12, B1-B10, and C1-C10, see Fig. 15A) from different instruction streams. Claims 10, 15, and 22 recite the corresponding limitations as set forth above in claim 3.

9. As to claim 4, Ito et al.'782 also discloses: the processor of claim 2 wherein execution of the instructions (such as A1-A12, B1-B10, and C1-C10, see Fig. 15A) is interleaved in a round-robin manner (see Fig. 15B). Claims 11, 16, and 23 recites the corresponding limitations as set forth above in claim 4.

10. As to claim 5, Ito et al.'782 also discloses: the processor of claim 1 wherein the processor ensures only one thread from the plurality of threads (Threads A, B, and C, see Figs. 3 and Fig. 15A) can handle an exception at any given time (see Col. 12, lines 17-23, regarding handling the exception in the Ito et al.'782's system and note one decoder (23a-23c) is handling one threat only see Fig. 1). Claim 17 recites the corresponding limitations as set forth above in claim 5.

11. As to claim 6, Ito et al.'782 also discloses: the processor of claim 1 further comprising a virtual memory addressing unit and a cache operable to store data communicated between the external interface (certainly existing in Ito et al.'782's system for handling input/output operation for peripherals) and the data path. Claim 18 recites the corresponding limitations as set forth above in claim 6.

12. As to claim 7, Ito et al.'782 also discloses: the processor of claim 1 wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a first and a second register (register parts 26a-26c, see Fig. 1) each containing a plurality of operands (such as source1 167 and source 2 and destination register No. 166, see Fig. 9 (a)-(c)), multiply (such as Fmult operation, see Col. 4, lines 31) the plurality of floating point operands (Fmult operation, see Col. 4, lines 31, using floating point operands) in the first register by the plurality of operands (such as source1 167 and source 2 and destination register No. 166, see Fig. 9 (a)-(c)) in the second register to produce a plurality of products and provide the plurality of products to partitioned fields of a result register (register parts 26a-26c, see Fig. 1) as a second catenated result. Note Claims 12, 19, and 24 recite the corresponding limitations as set forth above in claim 7.

Response to Arguments

13. Applicant's arguments filed 8 June 2007 have been fully considered but they are not persuasive.

14. Regarding claim 1, as stated in the rejection above, the single integer operation 164 is a single instruction acting on individual parts (bits). Integer operations such as addition and logical operations are functionally equivalent to performing operations on single bits (in the same way as is done in Applicants' invention).

15. Regarding claim 6, as shown in col. 5, lines 1-4, virtual addressing is described. Virtual addressing is merely transposing memory addresses corresponding with a program. The Load/Store unit is therefore a virtual memory addressing unit because it is capable of virtual memory addressing. There are no limitations in the claim to further limit the structure of said virtual memory addressing unit.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 10/1/2007

ALFORD KINDRED
PRIMARY EXAMINER